120

AF/2811

OIPE JAN 15 2004 PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

In re Patent Application of
TOKUSHIGE
Serial No. 09/660,926
Filed: September 13, 2000
Title: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

Atty Dkt. 900-348
C# M#
Group Art Unit: 2811
Examiner: Hu, S.
Date: January 15, 2004

RECEIVED
JAN 22 2004
TECHNOLOGY CENTER 2800

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

☐ **Correspondence Address Indication Form Attached.**

☐ **NOTICE OF APPEAL** Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the Examiner. ($ 330.00)	$	
☒ An appeal **BRIEF** is attached in triplicate in the pending appeal of the above-identified application ($ 330.00)	$	330.00
☐ Credit for fees paid in prior appeal without decision on merits	-$ (	)
☐ A reply brief is attached in triplicate under Rule 193(b)		**(no fee)**
☐ Petition is hereby made to extend the current due date so as to cover the filing date of this paper and attachment(s) (**$110.00/1 month**; $420.00/2 months; **$950.00/3 months**; $1480.00/4 months)	$	
SUBTOTAL	$	330.00
☐ Applicant claims "Small entity" status, enter ½ of subtotal and subtract ☐ "Small entity" statement attached.	-$(	)
SUBTOTAL	$	330.00
Less month extension previously paid on	-$(	0.00)
TOTAL FEE ENCLOSED	$	330.00

Any future submission requiring an extension of time is hereby stated to include a petition for such time extension. The Commissioner is hereby authorized to charge any deficiency, or credit any overpayment, in the fee(s) filed, or asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our **Account No. 14-1140.** A duplicate copy of this sheet is attached.

1100 North Glebe Road, 8th Floor
Arlington, Virginia 22201-4714
Telephone: (703) 816-4000
Facsimile: (703) 816-4100
JAR:caj

NIXON & VANDERHYE P.C.
By Atty: Joseph A. Rhoa, Reg. No. 37,515

Signature: _____

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of

TOKUSHIGE — Atty. Ref.: 900-348

Serial No. 09/660,926 — Group: 2811

Filed: September 13, 2000 — Examiner: Hu, S.

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

* *

January 15, 2004

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

Applicant hereby appeals to the Board of Patent Appeals and Interferences from the last decision of the Examiner.

REAL PARTY IN INTEREST

The real party in interest is Sharp Kabushiki Kaisha, a corporation of the country of Japan.

RELATED APPEALS AND INTERFERENCES

The appellant, the undersigned, and the assignee are not aware of any related appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Claims 1, 4-11 and 24 are pending and have been rejected. No claims have been substantively allowed. All of these claims are appealed herein.

STATUS OF AMENDMENTS

An Amendment After Final was filed October 20, 2003, and has been entered by the Examiner as evidenced by the Advisory Action dated November 13, 2003.

SUMMARY OF INVENTION

For purposes of example only and without limitation, certain example embodiments of this invention relate to a semiconductor device including both NMOS and PMOS transistors. For example, see the PMOS and NMOS transistors illustrates in Figs. 1(a)-(b).

Fig. 3 illustrates an example NMOS transistor. The semiconductor device shown in Fig. 3 comprises an NMOS transistor having source/drain regions 36 and being formed on a semiconductor layer 33 of an SOI substrate in which the semiconductor layer 33 is formed on a semiconductor substrate 31 of a first conductivity type with the intervention of a buried insulating film 32. Contact portion provided in contact hole 39a is provided for applying to the semiconductor substrate 31 different bias voltages in an operating state and a standby state of a semiconductor circuit including the transistor.

Impurity diffusion layer 31a of the first conductivity type is formed in the semiconductor substrate 31 under at least the entire source, drain and channel regions, so that the impurity diffusion layer 31a is of the same conductivity type as the

semiconductor substrate 31 (e.g., both P-type in Fig. 3). The contact portion provided in contact hole 39a applies the different bias voltages to substrate 31 via diffusion layer 31a and is formed in a device isolation region including insulating spacer 37a. Thus, a conductor of the contact portion in the contact hole 39a is electrically insulated from the semiconductor layer 33 by at least the device isolation region including dielectric 37a.

Moreover, in certain example embodiments, bias voltages applied to the different type transistors are changed between the active and standby states so that active regions of the first and second transistors (NMOS and PMOS transistors) are substantially completely depleted simultaneously in the standby state. Adjacent wells of the transistors may be electrically isolated from one another in certain example embodiments of this invention. This electrical isolation of adjacent wells is advantageous in that it permits much different bias voltages to be efficiently applied to the different wells thereby allowing active regions of the first and second transistors (NMOS and PMOS transistors) to be substantially completely depleted simultaneously in the standby state.

The electrical isolation of the contact portion from the semiconductor layer 33 is highly advantageous for a number of reasons. Because the contact portion and the semiconductor layer 33 are electrically insulated, the magnitude of the bias voltage may be controlled for each well when a number of wells are formed in the semiconductor substrate 31. Moreover, insulation of the contact from the semiconductor layer 33 also allows for the threshold value to be easily controlled by applying the voltage only from the well side. If the contact portion were not insulated from the semiconductor layer (as in Mitani), the charge in the S/D region tends to form a leak path from the well to the substrate via the contact thereby creating a well bias to be controlled depending upon an

ON/OFF state of the transistor. In contrast, insulation of the contact from the semiconductor layer according to certain embodiments of this invention allows for control of the threshold voltage of the transistor by applying different bias voltages depending upon an ON/OFF state thereby making it possible to realize a transistor having reduced leak path(s), less power consumption and/or higher controllability. Yet another advantage of electrically insulating the conductor of the contact portion from the semiconductor layer is that instability of current on switching the transistor can be reduced since the well bias may be controlled independent of the source/drain region.

ISSUES

1. Whether claims 1, 4-5, 7-9 and 11 are unpatentable under 35 U.S.C. Section 103(a) over Mitani (WO 99/27585 – see also US 6,392,277 for English text) in view of KR '470 (KR 96-12470).

2. Whether claims 6, 10 and 24 are unpatentable under 35 U.S.C. Section 103(a) over Mitani (WO 99/27585 – see also US 6,392,277 for English text) in view of both KR '470 (KR 96-12470) and Burr (US 6,072,217).[1]

GROUPING OF CLAIMS

The appealed claims are divided herein into the following separate and distinct groups, each of which is patentably distinct from the others.

Group A: Claims 1, 4 and 5.

Group B: Claim 6

Group C: Claims 7, 8, 9 and 11.

Group D: Claim 10.

Group E: Claim 24.

Each of the aforesaid groups is patentably distinct from all other groups for the reasons set forth below. For example, claim 6 (Group B) is patentably distinct from all other groups.

ARGUMENT

It is axiomatic that in order for a reference to anticipate a claim, it must disclose, teach or suggest each and every feature recited in the claim. See, e.g., Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983). The USPTO has the burden in this respect.

Moreover, the USPTO has the burden under 35 U.S.C. Section 103 of establishing a *prima facie* case of obviousness. In re Piasecki, 745, F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). It can satisfy this burden only by showing that some objective teaching in the prior art, or that knowledge generally available to one of ordinary skill in the art, would have led that individual to combine the relevant teachings of the references to arrive at the claimed invention. In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Before the USPTO may combine the disclosures of the references in order to establish a *prima facie* case of obviousness, there must be some suggestion for doing so. In re Jones, 958 F.2d 347 (Fed. Cir. 1992). Even

[1] The formality objections to claims 1, 4-11 and 24 set forth in Section/Paragraph 2 of the Final Rejection were addressed and overcome in the Amendment After Final filed October 20, 2003 which has been entered by the Examiner.

assuming, *arguendo*, that a given combination of references is proper, the combination of references must in any event disclose the features of the claimed invention in order to render it obvious.

I. Group A: Claim 1 (together with claims 4-5)

Claim 1 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Mitani in view of KR '470. Since the US counterpart to Mitani (i.e., Mitani '277) is in English, it is referred to herein for purposes of simplicity and understanding although the U.S. counterpart itself is not admitted to be prior art. This Section 103(a) rejection of claim 1 should be reversed for at least the following reasons.

Claim 1 requires that "the contact portion for applying the different bias voltages is formed in a device isolation region and comprises a contact hole in the semiconductor layer and the buried insulating film, said contact hole reaching the impurity diffusion layer so that the different bias voltages are applied to the substrate via the impurity diffusion layer, and wherein a conductor of the contact portion in the contact hole is electrically insulated from the semiconductor layer by at least said device isolation region which includes at least one insulator; and . . . . bias voltages applied via separate of said contact portion for the first transistor and a contact portion for the second transistor are changed between the active and standby states so that active regions of the first and second transistors are substantially completely depleted simultaneously in the standby state." For example, Fig. 3 of the instant application illustrates that conductor 37b of the contact portion in the contact hole is electrically isolated from semiconductor layer 33 by at least the device isolation region 37a and/or the like. Moreover, claim 1 also requires, for example, controlling the bias voltage for PMOS and NMOS transistors on the same

substrate between the active and standby state(s) so that active regions of the transistors are substantially completely depleted simultaneously in the standby state. The cited art fails to disclose or suggest each of the aforesaid underlined aspects of claim 1.

Mitani '277 (the US counterpart is referred to herein since it is in English) in Fig. 8 discloses an n-conduction type transistor Qn formed on semiconductor substrate 20A. The n-conduction type transistor Qn includes n-type source/drain regions 28 defined in the semiconductor layer, a p-type channel, gate insulator 22 and gate electrode 27 (e.g., see col. 9, line 65 to col. 10, line 11). A p-type region 24A is provided as a back gate. *Interconnect 33D provides interconnection between and supplies the same potential to both the semiconductor layer (region 31) and back gate 24A*. It can be seen that Mitani significantly differs from the invention of claim 1 in at least the following two respects.

First, as explained above, interconnect 33D in Fig. 8 of Mitani provides interconnection between and supplies the same potential to both the semiconductor layer (region 31) and back gate 24A. In other words, interconnect 33D is in electrical communication with both back gate 24A and the semiconductor layer of the SOI substrate, and is provided in order to supply the same electric potential to both. In direct contrast with Mitani, the invention of claim 1 intentionally *isolates* the contact for high concentration impurity diffusion layer 31a from the semiconductor layer of the SOI substrate via isolation region 37a. In this respect, claim 1 expressly states that "a conductor of the contact portion in the contact hole is electrically insulated from the semiconductor layer by at least said device isolation region which includes at least one insulator." Mitani fails to disclose or suggest this aspect of claim 1. Instead, Mitani

teaches directly away from this aspect of claim 1 by requiring that back gate 24A be electrically connected to the surface semiconductor layer via interconnect 33D.

Moreover, the recitation of the aforesaid "insulated" structure of claim 1 may provide for significant technical advantages over the undesirable structure of Mitani. Because the contact portion and the semiconductor layer are electrically insulated as recited in claim 1, the magnitude of the bias voltage may be controlled for each well when a number of wells are formed in the semiconductor substrate. Moreover, this "insulated" aspect of claim 1 also allows for the threshold value to be easily controlled by applying the voltage only from the well side. In contrast, Mitani because of the required electrical connection between 24A and 31 via interconnect 33D has very poor control over the threshold value since the same voltage is applied from both the back gate and the semiconductor layer. Mitani is highly undesirable in this respect.

Still further, when the contact portion is not insulated from the semiconductor layer (as in Mitani), the charge in the S/D region tends to form a leak path from the well to the substrate via the contact thereby creating a well bias to be controlled depending upon an ON/OFF state of the transistor. In contrast, the invention of claim 1 which electrically insulates the conductor of the contact portion from the semiconductor layer allows for control of the threshold voltage of the transistor by applying different bias voltages depending upon an ON/OFF state thereby making it possible to realize a transistor having reduced leak path(s), less power consumption and/or higher controllability. Yet another advantage of electrically insulating the conductor of the contact portion from the semiconductor layer is that instability of current on switching the transistor can be reduced since the well bias may be controlled independent of the

source/drain region. Thus, not only does Mitani fail to disclose or suggest electrically insulating the conductor of the contact portion from the semiconductor layer as required by claim 1, but Mitani is technically disadvantageous in this respect for the aforesaid reasons.

Second, Mitani fails to disclose or suggest that bias voltages are applied to first and second transistors Qn and Qp and are changed between the active and standby states so that active regions of both transistors are substantially *completely depleted simultaneously in the standby state* as called for in claim 1. The Office Action's contention that this is inherent is unsupported and lacks merit. The reference simply does not disclose or suggest this requirement of claim 1.

For each of the aforesaid reasons, it can be seen that Mitani is entirely unrelated to the invention of claim 1. Moreover, citation to KR '470 cannot overcome the aforesaid fundamental flaws of Mitani.

Additionally, *one of ordinary skill in the art would never have used the contact isolation region of KR '470 in Mitani because it would insulate the back gate contact from the semiconductor layer which would in turn destroy the functionality and purpose of Mitani*. Such a combination would clearly be improper under Section 103(a) as a matter of law, since Mitani expressly teaches that an electrical connection between the back gate and semiconductor layer should be provided thereby teaching directly away from the invention of claim 1. There is no suggestion in the art of record for the alleged combination. Moreover, even if such a combination were made (which applicant believes would be clearly incorrect), the invention of claim 1 still would not be met for the second reason discussed above.

II. Group B: Claim 6

Claim 6 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Mitani in view of KR '470 and/or Burr. This Section 103(a) rejection of claim 6 should be reversed for at least the following reasons.

Claim 6 requires that "the P-type well and the N-type well are formed in the semiconductor substrate and the *P-type well and the N-type well are substantially electrically isolated from each other.*" Electrical isolation of adjacent wells is advantageous in that it permits much different bias voltages to be efficiently applied to the different wells thereby allowing active regions of the first and second transistors (NMOS and PMOS transistors) to be efficiently substantially completely depleted simultaneously in the standby state in certain embodiments of this invention. The cited art fails to disclose or suggest this aspect of claim 6.

Mitani in Fig. 8 teaches directly away from this aspect of claim 6 because Mitani's back gates 24A and 24B (alleged P and N wells) contact one another and thus are not electrically isolated from each other. There is absolutely no suggestion in the art of record for isolating the two back gates of Mitani from one another.

The Examiner contends at the bottom of page 4 of the final rejection that this "electrically isolated" requirement of claim 6 is "inherent" in Mitani. The final rejection is wrong in this respect. As explained above, Mitani's back gates 24A and 24B (alleged P and N wells) contact one another and thus are not electrically isolated from each other. The Examiner's contention that this is "inherent" in Mitani is unsupported and lacks merit.

Burr is also not helpful in this regard. Burr relates to an entirely different type of device than does Mitani. Burr's adjacent transistors 702 and 704 are electrically isolated from one another via "Ox" provided therebetween. Since the overall transistors 702 and 704 are electrically isolated in Burr, it makes sense to also electrically isolate the two wells located beneath the respective transistors. However, in clear contrast with Burr, adjacent transistors in Fig. 8 of Mitani are not electrically isolated from one another. Instead, they share the same semiconductor material. In other words, Mitani and Burr utilize opposite types of structure. Thus, there is absolutely no reason why one of ordinary skill in the art would have electrically isolated that back gates 24A and 24B of Mitani as alleged in the final rejection. Burr's teaching is relevant only to devices where adjacent transistors are electrically isolated, and thus is not relevant to the structure of Mitani.

Accordingly, 3-way Section 103(a) rejection of claim 6 is incorrect and should be reversed.

III. Group C: Claim 7 (together with claims 8-9)

Claim 7 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Mitani in view of KR '470. This Section 103(a) rejection of claim 7 should be reversed for at least the following reasons.

Claim 7 requires that "a conductor of the contact portion in the contact region is electrically insulated from said semiconductor layer; and a second MOS transistor, wherein the first and second MOS transistors are of different conductivity types on the substrate, and wherein bias voltages applied via said contact portion for the first transistor and a separate contact region including a contact portion for the second transistor are

changed between the active and standby states so that active regions of the first and second transistors are substantially completely depleted simultaneously in the standby state." The cited art fails to disclose or suggest these aspects of claim 7.

As explained above, interconnect 33D in Fig. 8 of Mitani provides interconnection between and supplies the same potential to both the semiconductor layer (region 31) and back gate 24A. In other words, interconnect 33D is in electrical communication with both back gate 24A and the semiconductor layer of the SOI substrate, and is provided in order to supply the same electric potential to both. In direct contrast with Mitani, the invention of claim 7 intentionally *isolates* the contact for high concentration impurity diffusion layer 31a from the semiconductor layer of the SOI substrate via isolation region 37a. Mitani fails to disclose or suggest this aspect of claim 7. Instead, Mitani teaches directly away from this aspect of claim 7 by requiring that back gate 24A be electrically connected to the surface semiconductor layer via interconnect 33D.

Moreover, the recitation of the aforesaid "insulated" structure of claim 7 has significant example advantages which are discussed above with respect to claim 1.

Moreover, Mitani fails to disclose or suggest that active regions of both transistors are substantially *completely depleted simultaneously in the standby state* as called for in claim 7. The Office Action's contention that this is inherent is unsupported and lacks merit. The reference simply does not disclose or suggest this requirement of claim 7.

For each of the aforesaid reasons, it can be seen that Mitani is entirely unrelated to the invention of claim 7. Moreover, citation to KR '470 cannot overcome the aforesaid fundamental flaws of Mitani. Additionally, one of ordinary skill in the art would never have used the contact isolation region of KR '470 in Mitani because it would insulate the

back gate contact from the semiconductor layer which would in turn destroy the functionality and purpose of Mitani. Such a combination would clearly be improper under Section 103(a) as a matter of law, since Mitani expressly teaches that an electrical connection between the back gate and semiconductor layer should be provided thereby teaching directly away from the invention of claim 7. There is no suggestion in the art of record for the alleged combination. Moreover, even if such a combination were made (which applicant believes would be clearly incorrect), the invention of claim 7 still would not be met for the second reason discussed above.

IV. Group D: Claim 10

Claim 10 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Mitani in view of KR '470 and/or Burr. This Section 103(a) rejection of claim 10 should be reversed for at least the following reasons.

Claim 10 requires that "the P-type well and the N-type well are substantially electrically isolated from each other." Electrical isolation of adjacent wells is advantageous in that it permits much different bias voltages to be efficiently applied to the different wells thereby allowing active regions of the first and second transistors (NMOS and PMOS transistors) to be efficiently substantially completely depleted simultaneously in the standby state in certain embodiments of this invention. The cited art fails to disclose or suggest this aspect of claim 10.

Mitani in Fig. 8 teaches directly away from this aspect of claim 10 because Mitani's back gates 24A and 24B (alleged P and N wells) contact one another and thus are not electrically isolated from each other. There is absolutely no suggestion in the art of record for isolating the two back gates of Mitani from one another.

The Examiner contends at the bottom of page 4 of the final rejection that this "electrically isolated" requirement of claim 10 is "inherent" in Mitani. The final rejection is wrong in this respect. As explained above, Mitani's back gates 24A and 24B (alleged P and N wells) contact one another and thus are not electrically isolated from each other. The Examiner's contention that this is "inherent" in Mitani is unsupported and lacks merit.

Burr is also not helpful in this regard. Burr relates to an entirely different type of device than does Mitani. Burr's adjacent transistors 702 and 704 are electrically isolated from one another via "Ox" provided therebetween. Since the overall transistors 702 and 704 are electrically isolated in Burr, it makes sense to also electrically isolate the two wells located beneath the respective transistors. However, in clear contrast with Burr, adjacent transistors in Fig. 8 of Mitani are not electrically isolated from one another. Instead, they share the same semiconductor material. In other words, Mitani and Burr utilize opposite types of structure. Thus, there is absolutely no reason why one of ordinary skill in the art would have electrically isolated that back gates 24A and 24B of Mitani as alleged in the final rejection. Burr's teaching is relevant only to devices where adjacent transistors are electrically isolated, and thus is not relevant to the structure of Mitani.

Accordingly, 3-way Section 103(a) rejection of claim 10 is incorrect and should be reversed.

V. Group E: Claim 24

Claim 24 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Mitani in view of KR '470 and/or Burr. This Section 103(a) rejection of claim 24 should be reversed for at least the following reasons.

Claim 24 requires "the p-type and n-type wells being substantially isolated from one another; and respective contact portions for applying to the semiconductor substrate via the wells different bias voltages in a transistor operating state and a transistor standby state so that active regions of the different conductivity type transistors are substantially completely depleted simultaneously in the standby state, wherein said contact portions are electrically insulated from said semiconductor layer." The cited art fails to disclose or suggest these aspects of claim 24.

As explained above, interconnect 33D in Fig. 8 of Mitani provides interconnection between and supplies the same potential to both the semiconductor layer (region 31) and back gate 24A. In other words, interconnect 33D is in electrical communication with both back gate 24A and the semiconductor layer of the SOI substrate, and is provided in order to supply the same electric potential to both. In direct contrast with Mitani, the invention of claim 24 intentionally *isolates* the contact for high concentration impurity diffusion layer 31a from the semiconductor layer of the SOI substrate via isolation region 37a. Mitani fails to disclose or suggest this aspect of claim 24. Instead, Mitani teaches directly away from this aspect of claim 24 by requiring that back gate 24A be electrically connected to the surface semiconductor layer via interconnect 33D.

Moreover, the recitation of the aforesaid "insulated" structure of claim 24 has significant example advantages which are discussed above with respect to claim 1.

Moreover, Mitani fails to disclose or suggest that active regions of both transistors are substantially *completely depleted simultaneously in the standby state* as called for in claim 24. The Office Action's contention that this is inherent is unsupported and lacks merit. The reference simply does not disclose or suggest this requirement of claim 24.

It can be seen that Mitani is entirely unrelated to the invention of claim 24. Moreover, citation to KR '470 cannot overcome the aforesaid fundamental flaws of Mitani. Additionally, one of ordinary skill in the art would never have used the contact isolation region of KR '470 in Mitani because it would insulate the back gate contact from the semiconductor layer which would in turn destroy the functionality and purpose of Mitani. Such a combination would clearly be improper under Section 103(a) as a matter of law, since Mitani expressly teaches that an electrical connection between the back gate and semiconductor layer should be provided thereby teaching directly away from the invention of claim 24. There is no suggestion in the art of record for the alleged combination. Moreover, even if such a combination were made (which applicant believes would be clearly incorrect), the invention of claim 24 still would not be met for the second reason discussed above.

Furthermore, claim 24 also requires that the p-type and n-type wells are substantially isolated from one another. Electrical isolation of adjacent wells is advantageous in that it permits much different bias voltages to be efficiently applied to the different wells thereby allowing active regions of the first and second transistors (NMOS and PMOS transistors) to be efficiently substantially completely depleted simultaneously in the standby state in certain embodiments of this invention. The cited art fails to disclose or suggest this aspect of claim 24. Mitani in Fig. 8 teaches directly

away from this aspect of claim 24 because Mitani's back gates 24A and 24B (alleged P and N wells) contact one another and thus are not isolated from each other. There is absolutely no suggestion in the art of record for isolating the two back gates of Mitani from one another.

The Examiner contends at the bottom of page 4 of the final rejection that this "electrically isolated" requirement of claim 24 is "inherent" in Mitani. The final rejection is wrong in this respect. As explained above, Mitani's back gates 24A and 24B (alleged P and N wells) contact one another and thus are not electrically isolated from each other. The Examiner's contention that this is "inherent" in Mitani is unsupported and lacks merit.

Burr is also not helpful in this regard. Burr relates to an entirely different type of device than does Mitani. Burr's adjacent transistors 702 and 704 are electrically isolated from one another via "Ox" provided therebetween. Since the overall transistors 702 and 704 are electrically isolated in Burr, it makes sense to also electrically isolate the two wells located beneath the respective transistors. However, in clear contrast with Burr, adjacent transistors in Fig. 8 of Mitani are not electrically isolated from one another. Instead, they share the same semiconductor material. In other words, Mitani and Burr utilize opposite types of structure. Thus, there is absolutely no reason why one of ordinary skill in the art would have electrically isolated that back gates 24A and 24B of Mitani as alleged in the final rejection. Burr's teaching is relevant only to devices where adjacent transistors are electrically isolated, and thus is not relevant to the structure of Mitani.

Accordingly, 3-way Section 103(a) rejection of claim 24 is incorrect for the many reasons set forth above and should be reversed.

CONCLUSION

In conclusion it is believed that the application is in clear condition for allowance; therefore, early reversal of the Final Rejection and passage of the subject application to issue are earnestly solicited.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: _____
Joseph A. Rhoa
Reg. No. 37,515

JAR:caj
1100 North Glebe Road, 8th Floor
Arlington, VA 22201-4714
Telephone: (703) 816-4000
Facsimile: (703) 816-4100

APPENDIX

CLAIMS ON APPEAL

1. A semiconductor device comprising:

a first MOS transistor formed on a semiconductor layer of an SOI substrate in which the semiconductor layer is formed on a semiconductor substrate of a first conductivity type with the intervention of a buried insulating film,

a contact portion for applying to the semiconductor substrate different bias voltages in an operating state and a standby state of a semiconductor circuit including the first MOS transistor,

the first MOS transistor including source and drain regions of a second conductivity type, a channel of the first conductivity type, and wherein an impurity diffusion layer of the first conductivity type is formed in the semiconductor substrate under at least the entire source, drain and channel regions, so that the impurity diffusion layer is of the same conductivity type as the semiconductor substrate, wherein said source and drain regions as well as said channel are all formed in the semiconductor layer,

wherein the contact portion for applying the different bias voltages is formed in a device isolation region and comprises a contact hole in the semiconductor layer and the buried insulating film, said contact hole reaching the impurity diffusion layer so that the different bias voltages are applied to the substrate via the impurity diffusion layer, and wherein a conductor of the contact portion in the contact hole is electrically insulated from the semiconductor layer by at least said device isolation region which includes at least one insulator; and

a second MOS transistor, wherein the first and second MOS transistors are of different conductivity types on the substrate, and wherein bias voltages applied via separate of said contact portion for the first transistor and a contact portion for the second transistor are changed between the active and standby states so that active regions of the first and second transistors are substantially completely depleted simultaneously in the standby state.

4. A semiconductor device according to claim 1, wherein the impurity diffusion region is formed as a well in a surface of the semiconductor substrate which lies under the first MOS transistor, the well having an impurity concentration higher than that of the other region of the substrate, and the bias voltages are applied to the well.

5. A semiconductor device according to claim 4, wherein the well is a P-type well under an N-channel MOS transistor which is the first of said first and second MOS transistors, while a well for the other of the first and second MOS transistors is an N-type well formed in the semiconductor substrate under a P-channel MOS transistor which is the second of said first and second MOS transistors.

6. A semiconductor device according to claim 5, wherein a plurality of wells including the P-type well and the N-type well are formed in the semiconductor substrate and the P-type well and the N-type well are substantially electrically isolated from each other.

7. A semiconductor device comprising:

a first MOS transistor formed on a semiconductor layer of an SOI substrate in which the semiconductor layer is formed on a semiconductor substrate with the intervention of a buried insulating film,

an element isolating region formed in the semiconductor layer,

a contact region formed in the element isolating region for connection with a contact portion for applying a bias voltage to a well of the semiconductor substrate for the first MOS transistor, the well being of the first conductivity type same as that of the other region of the semiconductor substrate directly under the well;

wherein a conductor of the contact portion in the contact region is electrically insulated from said semiconductor layer; and

a second MOS transistor, wherein the first and second MOS transistors are of different conductivity types on the substrate, and wherein bias voltages applied via said contact portion for the first transistor and a separate contact region including a contact portion for the second transistor are changed between the active and standby states so that active regions of the first and second transistors are substantially completely depleted simultaneously in the standby state.

8. A semiconductor device according to claim 7, wherein the well is formed in a surface of the semiconductor substrate which lies under the first MOS transistor formed on the semiconductor layer, the well having an impurity concentration higher than that of the other region of the substrate, and the bias voltages are applied to the well.

9. A semiconductor device according to claim 8, wherein the well is a P-type well under an N-channel MOS transistor which is the first of said first and second MOS transistors, while a well for the other of the first and second MOS transistors is an N-type well formed in the semiconductor substrate under a P-channel MOS transistor which is the second of said first and second MOS transistors.

10. A semiconductor device according to claim 9, wherein a plurality of wells are formed in the semiconductor substrate and the P-type well and the N-type well are substantially electrically isolated from each other.

11. A semiconductor device according to claim 7, wherein different values of said bias voltages are applied in an operating state and a standby state of a semiconductor circuit including the at least the first MOS transistor, thereby to change a threshold voltage of at least the first MOS transistor.

24. A semiconductor device comprising:

a PMOS transistor and an NMOS transistor formed on a semiconductor layer of an SOI substrate in which the semiconductor layer is formed on a semiconductor substrate of a first conductivity type with the intervention of a buried insulating film,

a p-type well formed in the substrate for the NMOS transistor and an n-type well formed in the substrate for the PMOS transistor, the p-type and n-type wells being substantially isolated from one another; and

respective contact portions for applying to the semiconductor substrate via the wells different bias voltages in a transistor operating state and a transistor standby state so that active regions of the different conductivity type transistors are substantially completely depleted simultaneously in the standby state, wherein said contact portions are electrically insulated from said semiconductor layer.